Preliminary Specification

PRODUCT NUMBER: IE-TP20825664W10-1

CUSTOMER
APPROVED BY
DATE:

REVISION RECORD

REV.	REVISION DESCRIPTION	REV. DATE	REMARK
X01	INITIAL RELEASE	2023. 08. 15	
X02	Add the Panel electrical specification value	2023. 11. 17	Page 7、8
A01	Add the Module Weight Add the Packing Specification	2024. 01. 04	Page 5、18
A02	Modify OPERATING/STORAGR TEMP MODIFY RELIABILITY TEST TIME (120 hrs modify to 240hrs)	2024. 08. 06	Page 4, 16

CONTENTS

1. SCOPE

The purpose of this specification is to define the general provisions and quality requirements that apply to the supply of display cells. This document, is the highest level specification for this product. It describes the product, identifies supporting documents and contains specifications.

2. FEATURES

- Small molecular organic light emitting diode.
- Color : White
- Panel matrix : 256x64
- Driver IC : SSD1362
- Excellent quick response time.
- Extremely thin thickness for best mechanism design : 1.42 mm
- High contrast : 10,000:1
- Wide viewing angle : 160□
- Serial Peripheral Interface
- Strong environmental resistance.
- Wide range of operating temperature: -40 to 70°C.
- Polarizer .

3. MECHANICAL DATA

NO	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	256(W) x 64(H)	dot
2	Dot Size	0.174 (W) x 0.17 (H)	mm^2
3	Dot Pitch	0.198(W) x 0.194(H)	mm^2
4	Aperture Rate	77	%
5	Active Area	50.664(W) x 12.392 (H)	mm^2
6	Panel Size	60.6 (W) x 17.5 (H)	mm^2
7*	Panel Thickness	1.2 ± 0.12	mm
8	Module Size	95.6 (W) x17.5(H) x 1.42 (D)	mm^3
9	Diagonal A/A size	2.08	inch
10	Module Weight	2.92 ± 10%	gram

* Panel thickness includes substrate glass, cover glass and UV glue thickness.

4. MAXIMUM RATINGS

ITEM	MIN	MAX	UNIT	Condition	Remark
Logic Supply Voltage (V_{CI})	-0.3	5.5	V	Ta = 25°C	IC maximum rating
Supply Voltage (V_{CC})	-0.5	21	V	Ta = 25°C	IC maximum rating
Operating Temp.	-40	70	°C	-	-
Storage Temp	-40	85	°C	-	-

Note:

Maximum ratings are those values beyond which damages to the OLED module may occur. The OLED functional operation should be restricted to the limits in the section 6. Electrical Characteristics tables.

5. ELECTRICAL CHARACTERISTICS

5.1 D.C ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{CC}	Operating Voltage (for OLED panel)	Ta = 25°C	16	16.5	17	V
V_{CI}	Logic Supply Voltage	Ta = 25°C	1.65	-	3.5	V
V_{IH}	High Logic Input Level		0.8* V_{CI}	-	V_{CI}	V
V_{IL}	Low Logic Input Level		GND	-	0.2*V_{CI}	V

5.2 ELECTRO-OPTICAL CHARACTERISTICS PANEL ELECTRICAL SPECIFICATIONS

PARAMETER	MIN	TYP.	MAX	UNITS	COMMENTS
Normal mode current (ICC)		54	56	mA	100% pixels on (1)
	-	27.5	28.5		50% pixels on (1)
	-	12	13		20% pixels on (1)
Standby mode current consumption (ICC)	-	2	3	mA	Standby mode 10% pixels on (2)
Normal mode power consumption	-	891	924	mW	100% pixels on (1)
	-	454	471		50% pixels on (1)
	-	198	215		20% pixels on (1)
Standby mode power consumption		33	49.5	mW	Standby mode 10% pixels on (2)
ICC Sleep mode Current	-	-	10	uA	Sleep mode Current (3)
ICI Sleep mode Current	-	-	60	uA	Sleep mode Current (3)
Normal Luminance	200	250	-	cd/m^2	Display Average
Standby Luminance		50		cd/m^2	
CIEx (White)	0.26	0.30	0.34		x, y (CIE 1931)
CIEy (White)	0.29	0.33	0.37		
Dark Room Contrast	10,000:1				

(1) Normal mode condition :

- V_{CC} = 16.5V
- Contrast setting : 0xAC
- Duty setting : 1/64
- Frame rate: 105Hz

(2) Standby mode condition :

- V_{CC} = 16.5V
- Contrast setting : 0x2F
- Duty setting : 1/64
- Frame rate: 105Hz

(3) Sleep mode condition :

When send 0xAE command OLED display off and memory data will be maintained.

(4) Wake up condition :

When send 0xAF command OLED will be turned on.

Note: More setting refer to application note.

6. LIFETIME EXPECTANCY

ITEM	MIN	UNIT	Condition	Remark
Life Time (Operation)	10,000	Hrs	200 cd/m², 50% alternating checkerboard	Note (1)
Life Time (Operation)	7,000	Hrs	250 cd/m², 50% alternating checkerboard	Note (2)

Note:

a. Lifetime Expectancy is not guaranteed one but expected lifetime in normal condition

b. Under V_{CC} = 16.5V, Ta = 25°C, 50% RH.

c. Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.

(1) Setting of 200 cd/m^2:

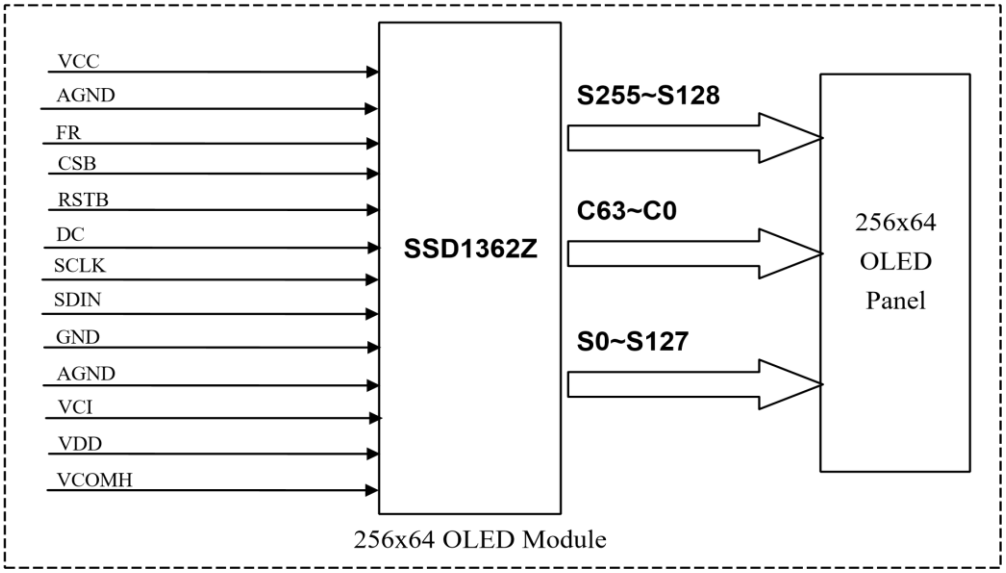
- Contrast setting : 0x8A
- Duty setting : 1/64

(2) Setting of 250 cd/m^2:

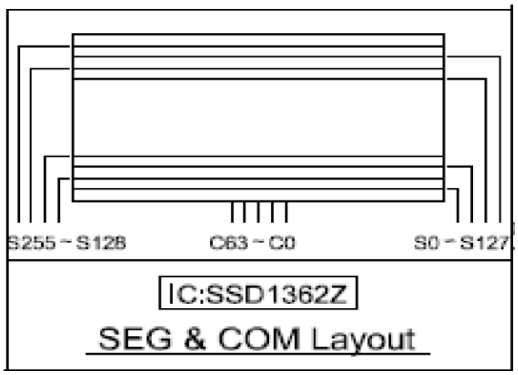
- Contrast setting : 0xAC
- Duty setting : 1/64

7. INTERFACE

7.1 FUNCTION BLOCK DIAGRAM



7.2 PANEL LAYOUT DIAGRAM



7.3 PIN ASSIGNMENTS

PIN No.	PIN Name.	DESCRIPTION	Setting at each interface		
			8080	SPI	IIC
1	VCC	Operating Voltage (for OLED panel)			
2	AGND	Analog system ground pin.			
3	FR	It should be kept NC if it is not used.			
4	CSB	This pin is the chip select input connecting to the MCU. (active LOW).		CS#	
5	RSTB	This pin is reset signal input.		Reset	
6	DC	This pin is Data/Command control pin connecting to the MCU.		D/C#	
7	SCLK	This pin is the serial clock input.		SCLK	
8	SDIN	This pin is the serial data input.		SDIN	
9	GND	Ground pin.			
10	AGND	Analog system ground pin.			
11	VCI	Logic Supply Voltage			
12	VDD	Power supply for core logic operation.			
13	VCOMH	COM signal deselected voltage level.			
14	VCC	Operating Voltage (for OLED panel)			

Note: Low is connected to GND High is connected to VCI

7.4 GRAPHIC DISPLAY DATA RAM ADDRESS MAP

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 256x64x4 bits. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. The GDDRAM address maps in Table show some examples on using the command “Set Remap” A0h to re-map the GDDRAM. In the following tables, the lower nibble and higher nibble of D0, D1, D2 … D8189, D8190, D8191 represent the 256x64 data bytes in the GDDRAM.

Table shows the GDDRAM map under the following condition:

- Command “Set Re -map” A0h is set to:
  - Disable Column Address Re-map (A[0]=0)
  - Disable Nibble Re-map (A[1]=0)
  - Enable Horizontal Address Increment (A[2]=0)
  - Disable COM Re-map (A[4]=0)
- Display Start Line=00h
- Data byte sequence: D0, D1, D2 … D8191

		SEG0	SEG1	SEG2	SEG3		SEG252	SEG253	SEG254	SEG255
		00		01			7E		7F	
COM0	00	D0[3:0]	D0[7:4]	D1[3:0]	D1[7:4]		D126[3:0]	D126[7:4]	D127[3:0]	D127[7:4]
COM1	01	D128[3:0]	D128[7:4]	D129[3:0]	D129[7:4]		D254[3:0]	D254[7:4]	D255[3:0]	D255[7:4]
⋮	⋮									
COM62	3E	D7936[3:0]	D7936[7:4]	D7937[3:0]	D7937[7:4]		D8062[3:0]	D8062[7:4]	D8063[3:0]	D8063[7:4]
COM63	3F	D8064[3:0]	D8064[7:4]	D8065[3:0]	D8065[7:4]		D8190[3:0]	D8190[7:4]	D8191[3:0]	D8191[7:4]
COM Outputs	Row Address (HEX)									

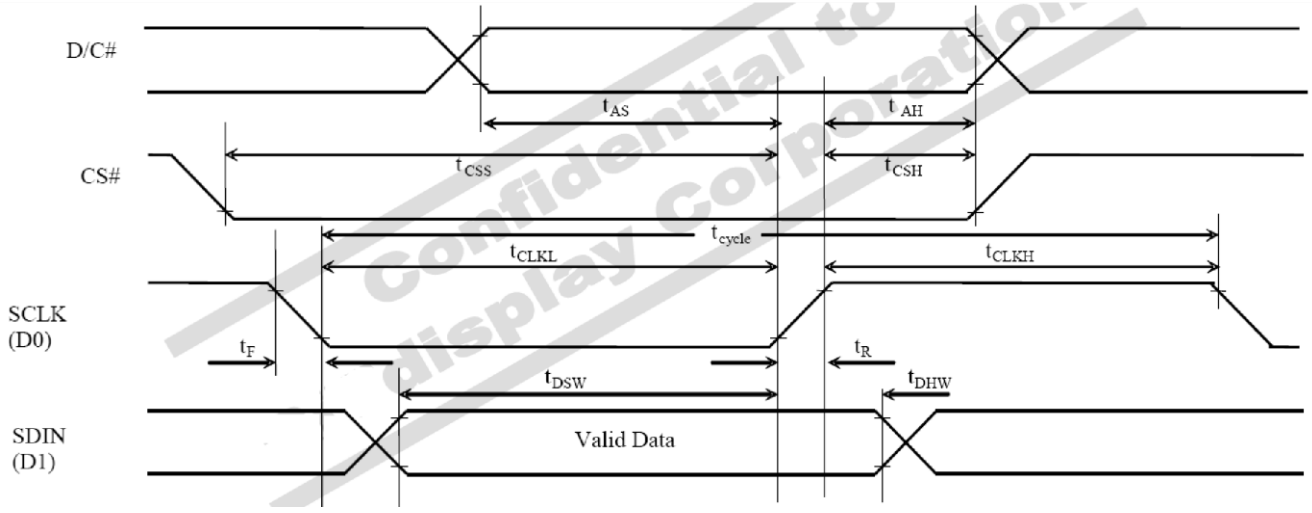
SEG Outputs Column Address (HEX)

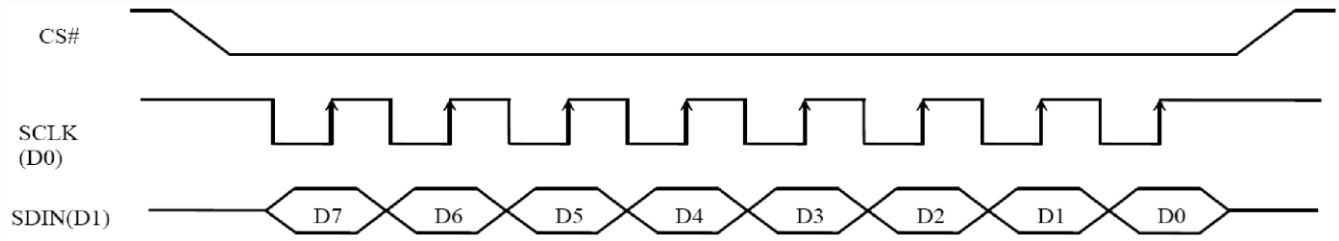
Nibble re-map A[1]=0

7.5 INTERFACE TIMING CHART(For 4-SPI)

V_{CI} - V_{SS} = 1.65V to 3.5V (T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	40	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	30	-	-	ns
t_{CLKL}	Clock Low Time	25	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns





8. POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT

8.1 POWER ON / OFF SEQUENCE

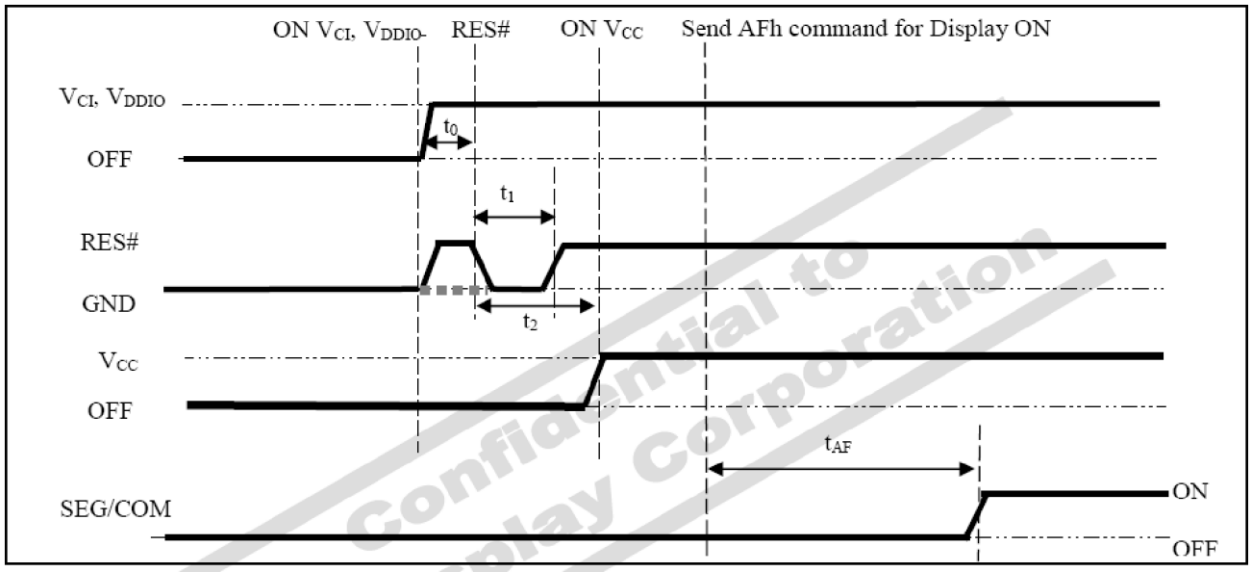
The following figures illustrate the recommended power ON and power OFF sequence of SSD1362 (assume VCI and VDDIO are at the same voltage level and internal VDD is used).

Power ON sequence:

1. Power ON VCI, VDDIO.
2. After VCI, VDDIO becomes stable, set wait time at least 1ms (t0) for internalVDD become stable. Then set RES# pin LOW (logic low) for at least 100us (t1)

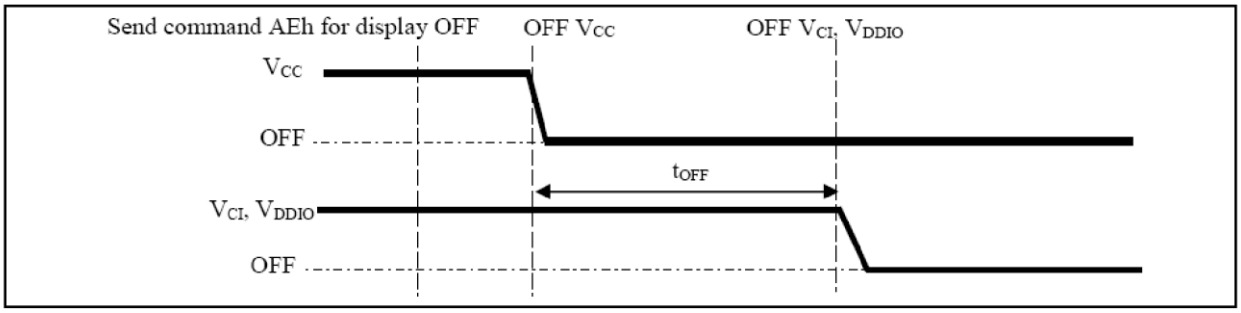
(4) and then HIGH (logic high).

3. After set RES# pin LOW (logic low), wait for at least 100us (t2). Then PowerON VCC.
4. After VCC become stable, send command AFh for display ON. SEG/COM willbe ON after 200ms (tAF).
5. After VCI, VDDIO become stable, wait for at least 50ms to send command.



Power OFF sequence:

1. Send command AEh for display OFF.
2. Power OFF VCC(1), (2)
3. Wait for tOFF. Power OFF VCI. (Typical tOFF=100ms(4))



Note:

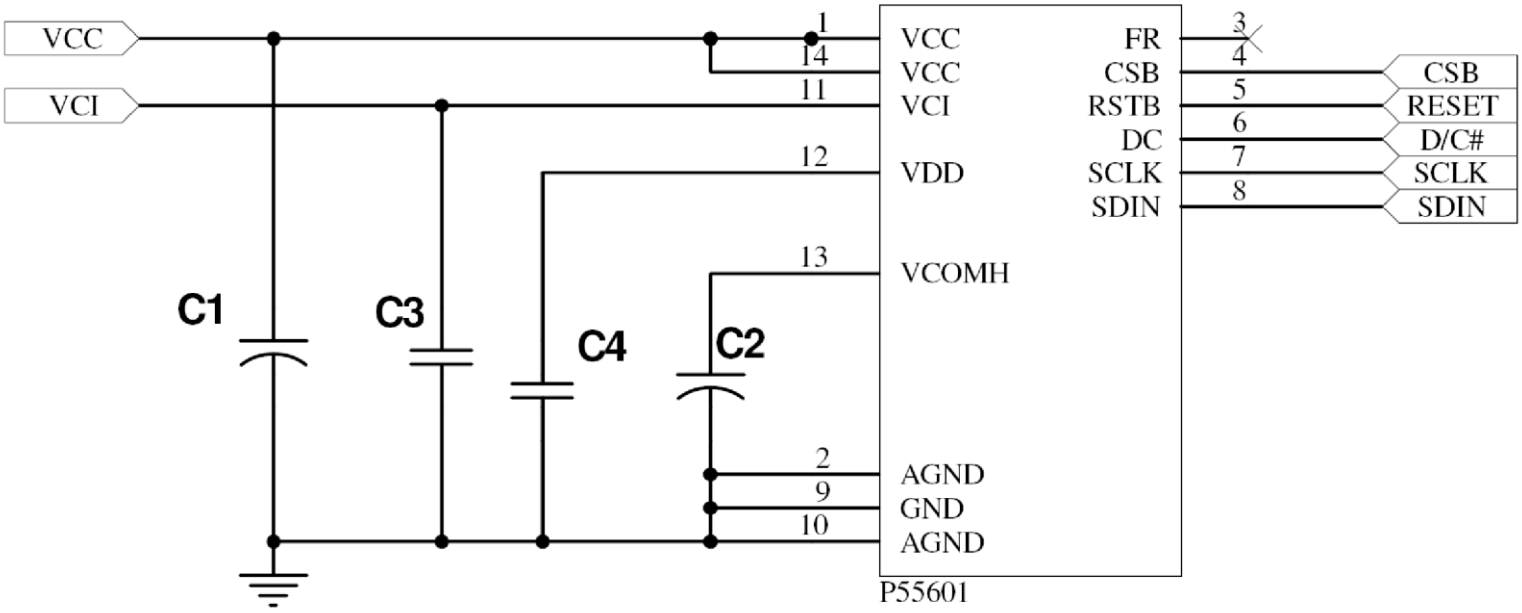
(1)VCC should be kept float (disable) when it is OFF.

(2) Power pins (VCI, VDDIO, VCC) can never be pulled to ground under any circumstance.

(3) The register values are reset after t1.

(4) VCI and VDDIO should not be Power OFF before VCC Power OFF.

8.2 APPLICATION CIRCUIT



Recommend components:

C1, C2 : 4.7uF/25V (Tantalum type) or VISHAY (572D475X0025A2T) C3, C4 : 1uF/16V(0603)

This circuit is for 4-SPI interface.

COMMAND TABLE

Refer to SSD1362 IC Spec.

9. RELIABILITY TEST CONDITIONS

No.	Items	Specification	Quantity
1	High temp. (Non-operation)	85°C, 240hrs	5
2	High temp. (Operation)	70°C, 120hrs	5
3	Low temp. (Operation)	-20°C, 120hrs	5
4	High temp. / High humidity (Operation)	65°C, 90%RH, 120hrs	5
5	Thermal shock (Nonoperation)	-40°C ~85°C (-40°C /30min; transit /3min; 85°C /30min; transit /3min) 1cycle: 66min, 100 cycles	5
6	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	1 Carton
7	Drop	Height: 80cm Sequence : 1 angle、3 edges and 6 faces Cycles: 1	1 Carton
8	ESD (Non-operation)	Air discharge model, ±8kV, 10 times	5

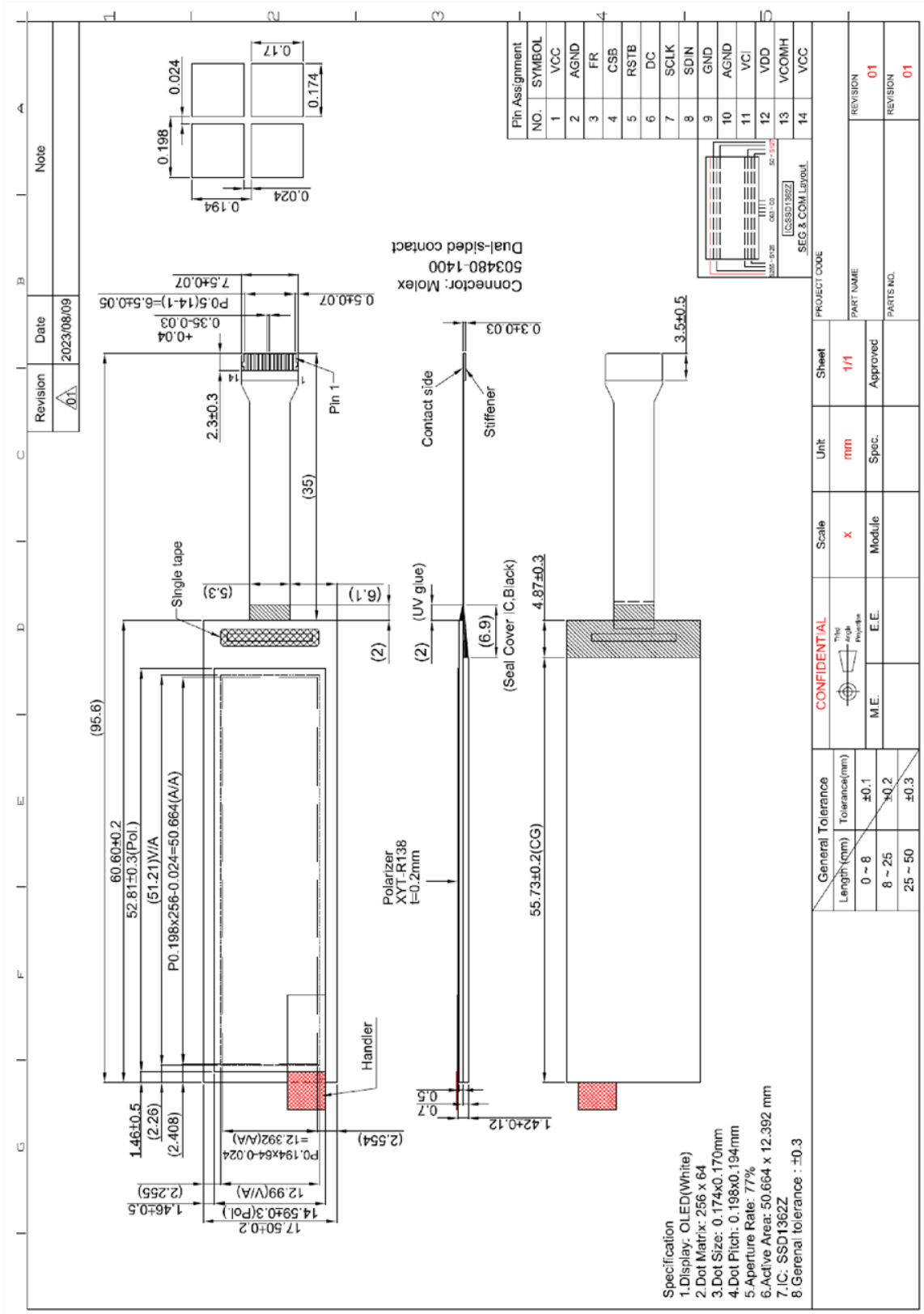
Test and measurement conditions

1. All measurements shall not be started until the specimens attain to temperature stability.
2. The degradation of Polarizer are ignored for item 1, 4 & 5.

Evaluation criteria 1. The function test is OK.

2. No observable defects.
3. Luminance: > 50% of initial value.
4. Current consumption: within ± 50% of initial value.

10. EXTERNAL DIMENSION



11. OUTGOING INSPECTION PROVISION

1. / SAMPLING METHOD

MIL-STD-1916 / inspection level III / normal inspection / single sample inspection

Major Level III ; Minor Level II

MIL-STD-1916樣本代字對照表							
批量	驗證水準（VL）						
	VII	VI	V	IV	III	II	I
2～170	A	A	A	A	A	A	A
171～288	A	A	A	A	A	A	B
289～544	A	A	A	A	A	B	C
545～960	A	A	A	A	B	C	D
961～1632	A	A	A	B	C	D	E
1633～3072	A	A	B	C	D	E	E
3073～5440	A	B	C	D	E	E	E
5441～9216	B	C	D	E	E	E	E
9217～17408	C	D	E	E	E	E	E
17409～30720	D	E	E	E	E	E	E
≧30721	E	E	E	E	E	E	E

Sample Code (CL)	Verification Level (VL)							
	T	VII	VI	V	IV	III	II	I
	Sample size							
A	3072	1280	512	192	80	32	12	5
B	4096	1536	640	256	96	40	16	6
C	5120	2048	768	320	128	48	20	8
D	6144	2560	1024	384	160	64	24	10
E	8192	3072	1280	512	192	80	32	12

2. INSPECTION CONDITION

The inspection and meaurement are performed under the following conditions, unless otherwise specified.

Temperature: 25±5°C / Humidity: 45±15%R.H.

Pressure: 860~1060hPa (mbar)

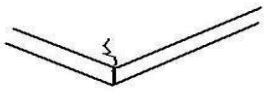
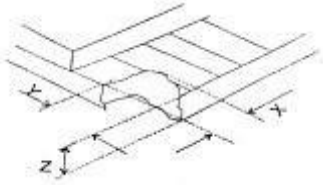
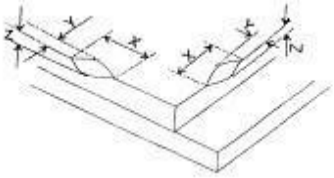
Distance between the panel and eyes of the inspector≧30cm

3. SPECIFICATION FOR QUALITY CHECK

3.1 DEFECT CLASSIFICATION

Severity	Inspection Item	Defect	Remark
Major Defect	1. Panel	(1) Non-displaying	
		(2) Line defects	
		(3) Malfunction	
		(4) Glass cracked	
	2. Film	(1) Film dimension out of specification	Can not be assembled
	3. Dimension	(1) Outline dimension o ut of specification	
Minor Defect	1.Panel	(1) Glass scratch	Appearance defect
		(2) Glass cutting NG	
		(3) Glass chip	
	2.Polarizer	(1) Polarizer scratch	
		(2) Stains on surface	
		(3) Polarizer bubbles	
	3. Displaying	(1) Dim spot、Bright spot、dust	
	4. Film	(1) Damage	
		(2) Foreign material	

3.2 出貨規格 / OUTGOING SPECIFICATION

<table>
<tr><th>Item</th><th>Description</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>I. Panel</td><td>1.Glass scratch</td><td>
<table>
<tr><th>Width
(mm)
W</th><th>Length
(mm)
L</th><th>number of pieces permitted</th></tr>
<tr><td>W≦0.05</td><td>Ignore</td><td>Ignore</td></tr>
<tr><td>0.05 ﹤ W≦0.1</td><td>L≦5</td><td>3</td></tr>
<tr><td>0.1 ﹤ W</td><td>------</td><td>None</td></tr>
<tr><td>beyond A.A.</td><td>------</td><td>Ignore</td></tr>
</table>
</td><td>Minor</td></tr>
<tr><td></td><td>2. Glass crack</td><td>(1) Crack 。
Propagation crack is not acceptable.
  </td><td>Major</td></tr>
<tr><td></td><td>3. Glass chip</td><td>(1) / Chip on corner
 
(2) / Chip on edge
  </td><td>Minor</td></tr>
</table>

<table>
<tr><th>Item</th><th>Description</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>I. Panel</td><td>3. Glass chip</td><td>Pretermission when no influence on Display Function.</td><td>Minor</td></tr>
<tr><td></td><td>4. Dimension</td><td>Refer to the drawing of the spec</td><td>Major</td></tr>
<tr><td>II. Polarizer</td><td>1. Scratch</td><td>Spot type in accordance with the criteria of “Item II-3. Polarizer bubble”. Line type in accordance with the criteria of “Item I-1. Glass scratch”.</td><td>Minor</td></tr>
<tr><td></td><td>2. Stains on surface</td><td>Stains cannot be removed even when wiped lightly with a soft cloth or similar cleaning.</td><td>Minor</td></tr>
<tr><td></td><td>3. Polarizer bubble</td><td>(mm)<table><tr><th>Size</th><th>number of pieces permitted</th></tr><tr><td>Φ≦0.2</td><td>Ignore</td></tr><tr><td>0.2＜Φ≦0.5</td><td>3</td></tr><tr><td>0.5＜Φ</td><td>0</td></tr><tr><td>beyond A.A.</td><td>Ignor</td></tr></table></td><td>Minor</td></tr>
</table>

<table>
<tr><th>Item</th><th>Description</th><th>Criterion</th><th>AQL</th></tr>
<tr><td rowspan="5">III. Displaying</td><td>1. Power consumption</td><td>The module operating current consumption should not go beyond the standard indicated in Product Specification</td><td>Major</td></tr>
<tr><td>2. Pixel size</td><td>The tolerance of display pixel dimension should be within ±25% of specification.</td><td>Minor</td></tr>
<tr><td>3.Color</td><td>Refer to the product specification.</td><td>Major</td></tr>
<tr><td>4. Luminance</td><td>Refer to the product specification.</td><td>Major</td></tr>
<tr><td>5. Dimming spot
Lighting spot
Dust</td><td>1.
<table>
<tr><th>Average diameter D:(mm)</th><th>number of pieces permitted</th></tr>
<tr><td>D ≦0.1</td><td>Ignore</td></tr>
<tr><td>0.1 < D ≦ Pixel Pitch</td><td>3</td></tr>
<tr><td>Pixel Pitch < D</td><td>0</td></tr>
<tr><td>beyond A.A.</td><td>Ignore</td></tr>
</table>
D=(long diameter + short diameter)

Pixel off is not allowed.</td><td>Minor</td></tr>
</table>

<table>
<tr><th>Item</th><th>Description</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>III. Displaying</td><td>5. Dimming spot
Lighting spot
Dust</td><td>2.
<table>
<tr><th>width(mm) W</th><th>length(mm) L</th><th>number of pieces permitted</th></tr>
<tr><td>W≦0.05</td><td>Ignore</td><td>Ignore</td></tr>
<tr><td>0.05 ﹤ W≦0.1</td><td>L≦2</td><td>3</td></tr>
<tr><td>0.1 ﹤ W</td><td>------</td><td>None</td></tr>
<tr><td>beyond A.A.</td><td>------</td><td>Ignore</td></tr>
</table></td><td>Minor</td></tr>
<tr><td>IV. Film</td><td>1. Dimension</td><td>Film dimension out of Spec.</td><td>Major</td></tr>
<tr><td></td><td>2. Damage</td><td>Crack; deep scratch; deep fold; deep pressure mark or other damage is not acceptable.</td><td>Minor</td></tr>
<tr><td></td><td>3. Foreign material</td><td>Conductive foreign material sticking to the leads, foreign material between film and glass are not acceptable.</td><td>Minor</td></tr>
</table>

12. APPENDIXES

APPENDIX 1: DEFINITIONS

A. DEFINITION OF CHROMATICITY COORDINATE

The chromaticity coordinate is defined as the coordinate value on the CIE 1931 color chart for R, G, B, W.

B. DEFINITION OF CONTRAST RATIO

The contrast ratio is defined as the following formula:

$$\text{Contrast Ratio} = \frac{\text{Luminance of all pixels on measurement}}{\text{Luminance of all pixels off measurement}}$$

C. DEFINITION OF RESPONSE TIME

The definition of turn-on response time Tr is the time interval between a pixel reaching 10% of steady state luminance and 90% of steady state luminance. The definition of turn-off response time Tf is the time interval between a pixel reaching 90% of steady state luminance and 10% of steady state luminance. It is shown in Figure 2.

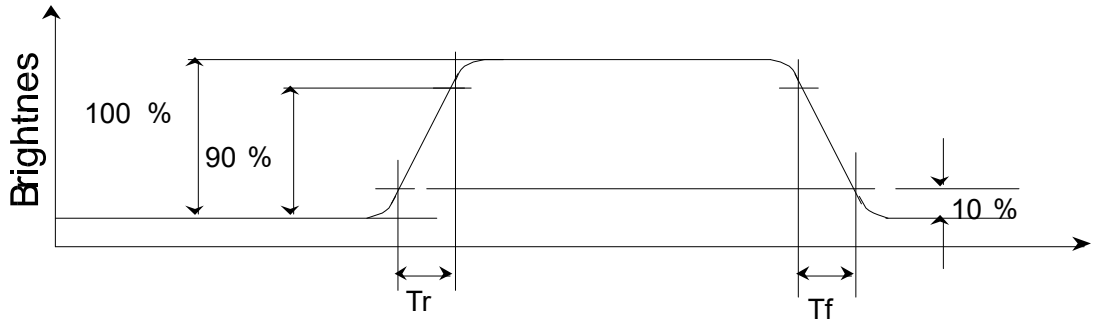


Figure 2: Response time

D. DEFINITION OF VIEWING ANGLE

The viewing angle is defined as Figure 3. Horizontal and vertical (H & V) angles are determined for viewing directions where luminance varies by 50% of the perpendicular value.

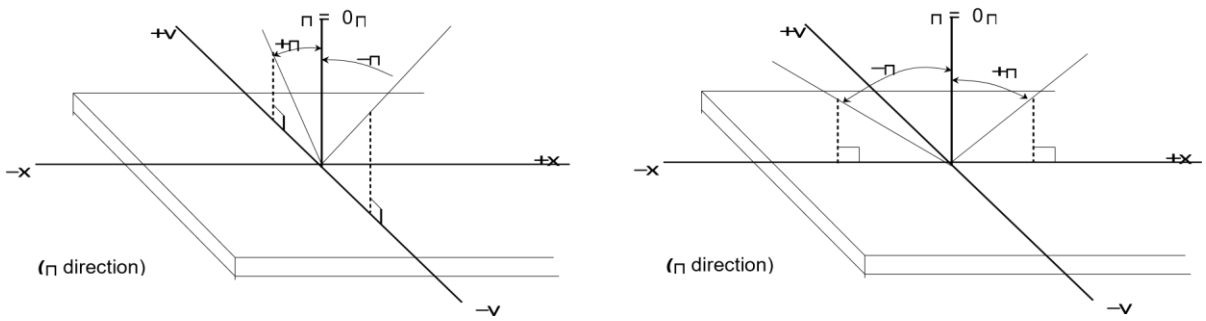
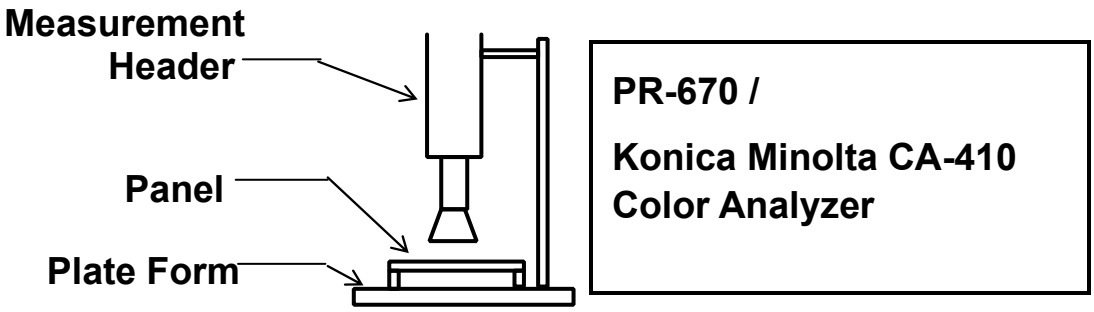


Figure 3: Viewing Angle

APPENDIX 2: MEASUREMENT APPARATUS

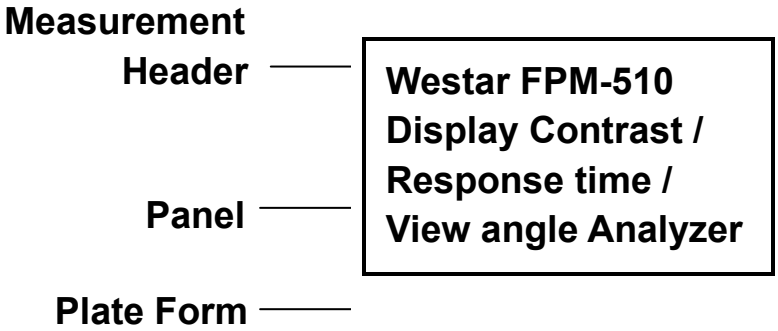
A. LUMINANCE/COLOR COORDINATE

PHOTO RESEARCH PR-670, Konica Minolta CA-410



B. CONTRAST / RESPONSE TIME / VIEW ANGLE

WESTAR CORPORATION FPM-510



C. ESD ON AIR DISCHARGE MODE