PRODUCT SPECIFICATIONS

For Customer: _____ ☐ : APPROVAL FOR SPECIFICATION

Customer Model No. _____ ☐ : APPROVAL FOR SAMPLE

Module No.: *IE-A-1918CV04MP-C0-1* *Date : 2022-11-05*

Table of Contents

For Customer's Acceptance:

Approved By	Comment

PREPARED	CHECKED	VERIFIED BY QA DEPT	VERIFIED BY R&D DEPT
Wu			

2. Revision Record

Date	Rev. No.	Page	Revision Items	Prepared
2022-11-05	V0		The first release.	Wu

3. General Specifications

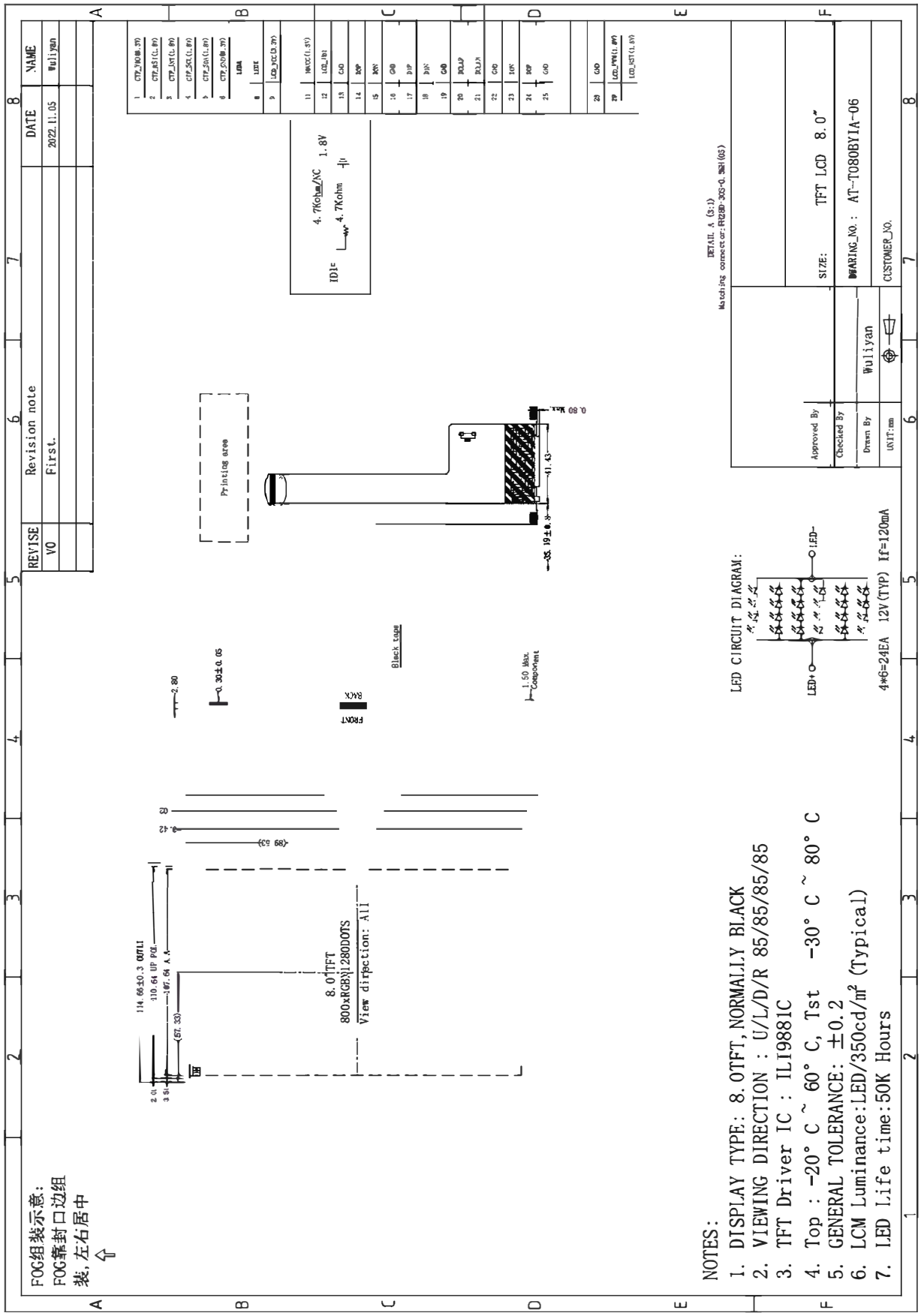
AT-T080BYIA-06 is a TFT-LCD module. It is composed of a TFT-LCD panel, driver IC, FPC,a back light unit. The 8.0″ display area contains 800 x (RGB) x 1280 *pixels and can display up to 16.7M colors. This product accords with ROHS environmental criterion.*

Item	Contents	Unit	Note
LCD Type	TFT	-	
Display color	16.7M	-	1
Viewing Direction	ALL	O'Clock	
Operating temperature	-20~+60	℃	
Storage temperature	-30~+80	℃	
Module size	114.66X184.16X2.8	mm	2
Active Area(W×H)	107.64X172.22	mm	
Number of Dots	800 x (RGB)x 1280	dots	
LCM Controller	ILI9881C	-	
Power Supply Voltage	3.3	V	
Backlight	4S6P-LEDs (white)	pcs	
Weight	---	g	
Interface	MIPI	-	

Note 1: Color tune is slightly changed by temperature and driving voltage.

Note 2: Without FPC and Solder.

4.Outline.Drawing



5. Absolute Maximum Ratings(Ta=25℃)

5.1 Electrical Absolute Maximum Ratings.(Vss=0V , Ta=25℃)

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	VCC	2.5	3.6	V	1，2
	IOVCC	1.8	3.6	V	1，2

Notes:

1. If the module is above these absolute maximum ratings. It may become permanently damaged. Using the module within the following electrical characteristic conditions are also exceeded, the module will malfunction and cause poor reliability.
2. V_{CC} >V_{SS} must be maintained.

5.2 Environmental Absolute Maximum Ratings.

Item	Storage		Operating		Note
	MIN.	MAX.	MIN.	MAX.	
Ambient Temperature	-30℃	80℃	-20℃	60℃	1,2
Humidity	-	-	-	-	3

1. The response time will become lower when operated at low temperature.

2. Background color changes slightly depending on ambient temperature.
The phenomenon is reversible.

3. Ta<=40℃:85%RH MAX.
Ta>=40℃:Absolute humidity must be lower than the humidity of 85%RH at 40℃.

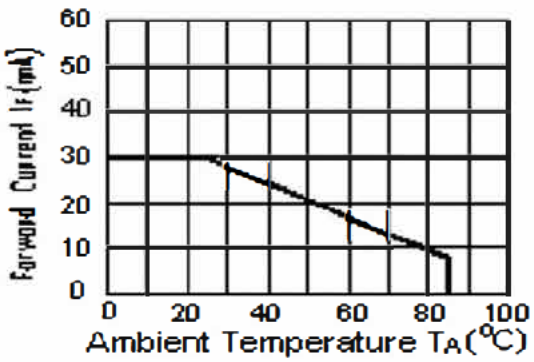
6. Electrical Specifications

6.1 Electrical characteristics(Vss=0V , Ta=25℃)

Parameter		Symbol	Condition	Min	Typ	Max	Unit	Note
Power supply		VCC	Ta=25℃	2.8	3.3	3.6	V	
		IOVCC	Ta=25℃	-	1.8	3.3	V	
Input voltage	'H'	V_{IH}	Ta=25℃	0.8*IOVCC	-	IOVCC	V	
	'L'	V_{IL}	Ta=25℃	0	-	0.2*IOVCC	V	

6.2 LED backlight specification(VSS=0V ,Ta=25℃)

Item	Symbol	Condition	Min	Typ	Max	Unit	Note
Supply voltage	Vf	If=120mA	10.8	12.0	13.2	V	
Uniformity	ΔBp	If=120mA	75	80	-	%	
Life Time	time	If=120mA	-	50K		hours	1



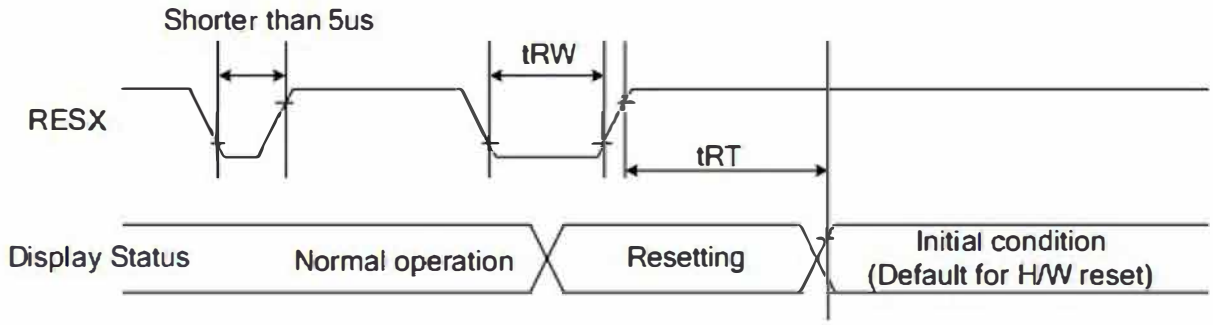
Note 1: Brightness to be decreased to 50% of the initial value at ambient temperature TA=25℃

6.3 Interface signals

Pin No.	Symbol	I/O	Function
1	CTP_VDD	P	CTP Power supply
2	CTP_RST	I	CTP reset pin
3	CTP_INT	I/O	External Interrupt to the IC of CTP
4	CTP_SCL	I	I2C clock
5	CTP_SDA	I/O	I2C data
6	CTP_GND	P	CTP Ground.
7	LEDA	P	LED Anode.
8	LEDK	P	LED Cathode.
9	LCD_VCC	P	Power supply
10	GND	P	Ground.
11	IOVCC	-	Power supply for IO
12	LCD_ID1	O	ID PIN
13	GND	P	Ground.
14	D3P	I	MIPI-DSI Data differential signal input pins. (Data lane 3)
15	D3N	I	MIPI-DSI Data differential signal input pins. (Data lane 3)
16	GND	P	Ground.
17	D1P	I	MIPI-DSI Data differential signal input pins. (Data lane 1)
18	D1N	I	MIPI-DSI Data differential signal input pins. (Data lane 1)
19	GND	P	Ground.
20	DCLKP	I	MIPI-DSI CLOCK differential signal input pins.
21	DCLKN	I	MIPI-DSI CLOCK differential signal input pins.
22	GND	P	Ground.
23	D0N	I	MIPI-DSI Data differential signal input pins. (Data lane 0)
24	D0P	P	MIPI-DSI Data differential signal input pins. (Data lane 0)
25	GND	I	Ground.
26	D2P	I	MIPI-DSI Data differential signal input pins. (Data lane 2)
27	D2N	I	MIPI-DSI Data differential signal input pins. (Data lane 2)
28	GND	P	Ground.
29	LCD_PWM	O	PWM Signal,1 for high luminance, 0 for low luminance
30	LCD_RST	I	Reset pin,active “L”

6.4 AC Characteristics

Reset Timing



Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

Notes:

1. *The reset cancel also includes required time for loading ID bytes, VCOM setting and other settings from EEPROM to registers. This loading is done every time when there is H/W reset cancel time (tRT) within 5 ms after a rising edge of RESX.*
2. *Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the Table 48.*

Table 48: Reset Descript

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

3. During the Resetting period, the display will be blanked (The display enters the blanking sequence, which maximum time is 120 ms, when Reset Starts in the Sleep Out mode. The display remains the blank state in the Sleep In mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection can also be applied during a valid reset pulse, as shown below:

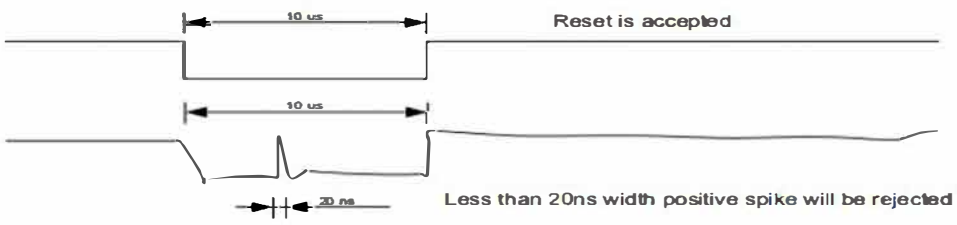
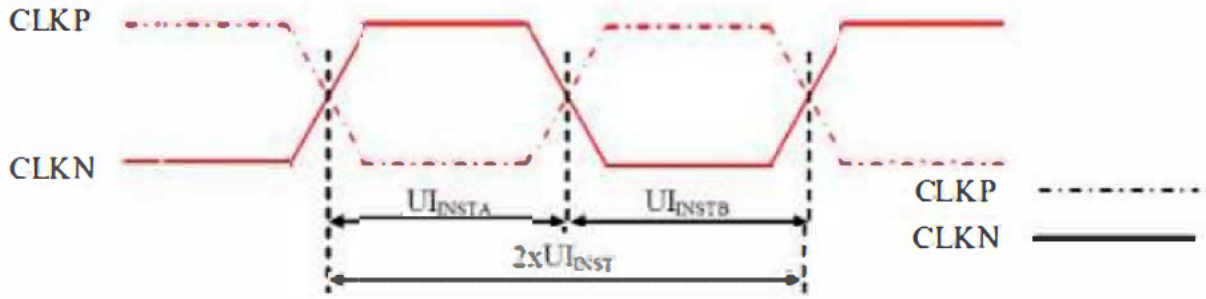


Figure 125: Positive Noise Pulse during Reset Low

5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

High Speed Mode – Clock Channel Timing



Signal	Symbol	Parameter	Min	Max	Unit
CLKP/N	$2xUI_{INST}$	Double UI instantaneous	*Note 2*	25	ns
CLKP/N	UI_{INSTA}, UI_{INSTB} (Note 1)	UI instantaneous Half	*Note 2*	12.5	ns

Notes:

1. UI = UIINSTA = UIINSTB

2. Define the minimum value, see Table 39.

Table 39: Limited Clock Channel Speed

Data type	Two Lanes speed	Three Lanes speed	Four Lanes speed
Data Type = 00 1110 (0Eh), RGB 565, 16 UI per Pixel	566 Mbps	466 Mbps	366 Mbps
Data Type = 01 1110 (1Eh), RGB 666, 18 UI per Pixel	637 Mbps	525 Mbps	412 Mbps
Data Type = 10 1110 (2Eh), RGB 666 Loosely, 24 UI per Pixel	850 Mbps	700 Mbps	550 Mbps
Data Type = 11 1110 (3Eh), RGB 888, 24 UI per Pixel	850 Mbps	700 Mbps	550 Mbps

High Speed Mode – Data Clock Channel Timing

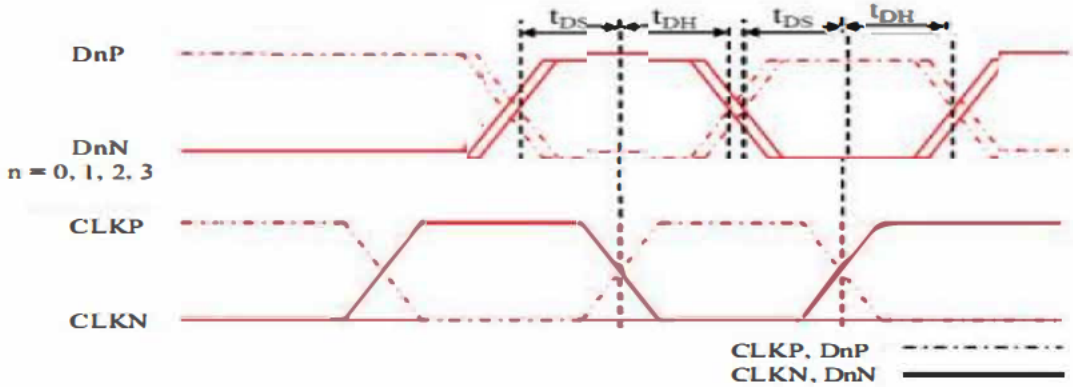
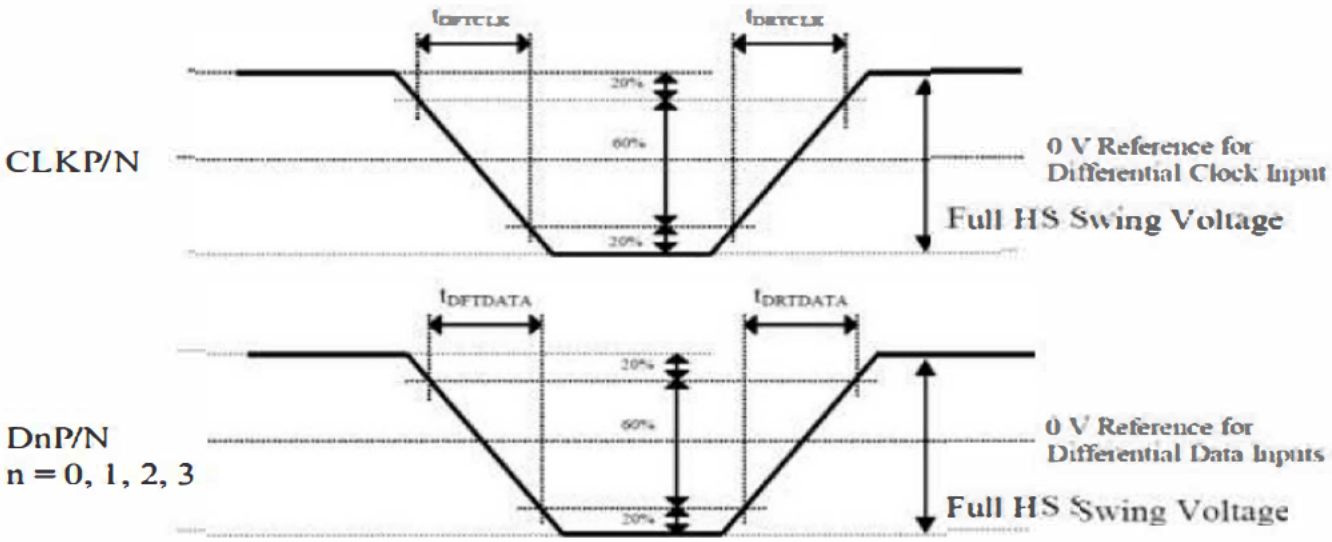


Figure 117: DSI Data to Clock Channel Timings

Table 40: DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min	Max
DnP/N , n=0 and 1	t_{DS}	Data to Clock Setup time	0.15xUI	-
	t_{DH}	Clock to Data Hold Time	0.15xUI	-

High Speed Mode – Rising and Falling Timings



Parameter	Symbol	Condition	Specification		
			Min	Typ	Max
Differential Rise Time for Clock	t_{DRTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Rise Time for Data	$t_{DRTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)
Differential Fall Time for Clock	t_{DFTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Fall Time for Data	$t_{DFTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)

Note: *The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-Phy standard.*

Data-Clock Timing Specifications

The Data-Clock timing specifications are shown in Table 13.12. Implementers shall specify a value $UI_{INST,MIN}$ that represents the minimum instantaneous UI possible within a High-Speed data transfer for a given implementation. Parameters in Table 13.12 are specified as a part of this value.. The setup and hold times, $T_{SETUP[RX]}$ and $T_{HOLD[RX]}$, respectively, describe the timing relationships between the data and clock signals. $T_{SETUP[RX]}$ is the minimum time that data shall be present before a rising or falling clock edge and $T_{HOLD[RX]}$ is the minimum time that data shall remain in its current state after a rising or falling clock edge. The timing budget specifications for a receiver shall represent the minimum variations observable at the receiver for which the receiver will operate at the maximum specified acceptable bit error rate.

The intent in the timing budget is to leave $0.4*UI_{INST}$, i.e. $\pm 0.2*UI_{INST}$ for degradation contributed by the interconnect.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Data to Clock Setup Time [RX]	$T_{SETUP[RX]}$	0.15	-	-	UIINST	1
Clock to Data Hold Time [RX]	$T_{HOLD[RX]}$	0.15	-	-	UIINST	1

Note: (1) Total setup and hold window for receiver of 0.3*UIINST.

Burst Mode Data Transmission

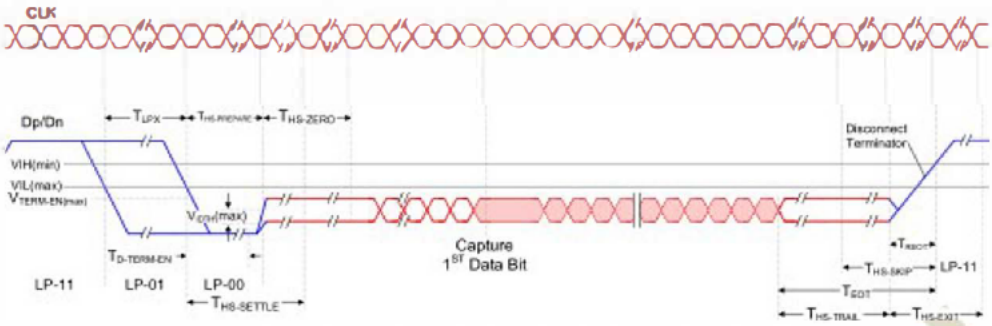
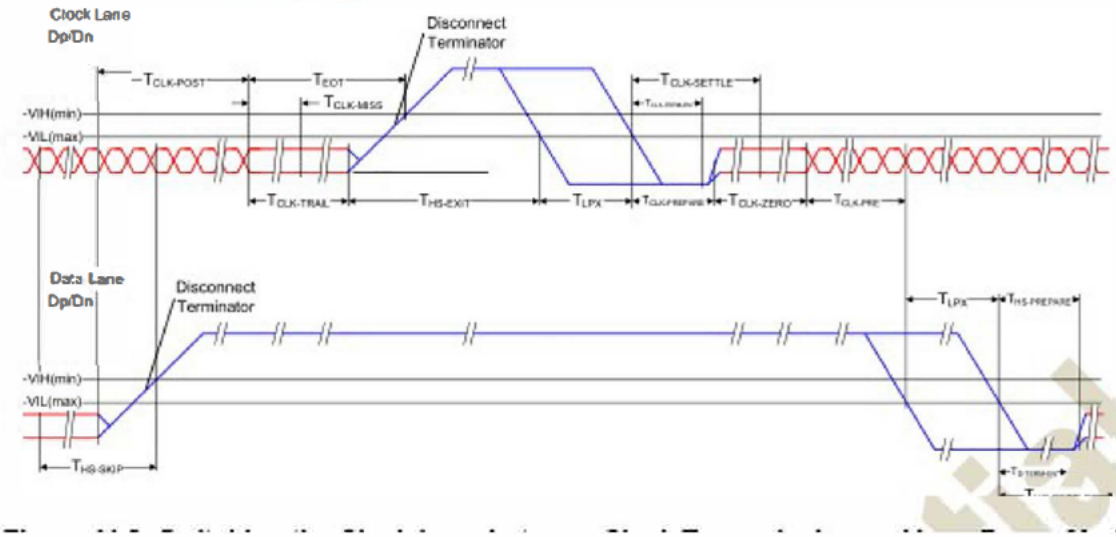


Figure 11.7: High-Speed Data Transmission in Bursts

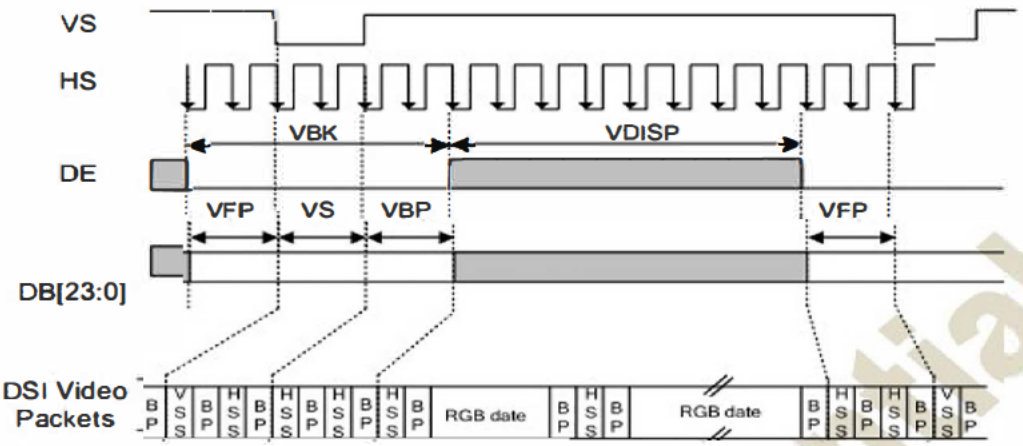
Parameter	Description	Min	Typ	Max	UNIT
T_{LPX}	Transmitted length of any Low-Power state period	50	-	-	ns
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40 + 4*UI	-	85 + 6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145 + 10*UI	-	-	ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination.	-	-	35 + 4*UI	ns
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions.	85 + 6*UI	-	145 + 10*UI	ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	max(n*8*UI, 60 + n*4*UI)	-	-	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100	-	-	ns



Parameter	Description	Min	Typ	Max	UNIT
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode.	60 + 52*UI	-	-	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8*UI	-	-	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38	-	95	ns
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300	-	-	ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination.	-	-	38	ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60	-	-	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100	-	-	ns

Timings for DSI Video mode

Vertical Timings



Resolution=800x1280(T_A=25°C, IOVCC=1.8V, VCIP=2.8V, VCI=2.8V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical low pulse width	VS	-	2	4	200 Note(1)	Line
Vertical front porch	VFP	-	4	20	200	Line
Vertical back porch	VBP	-	2	10	200 Note(1)	Line
Vertical blanking period	VBK	VS+VBP+VFP	8	34	250	Line
Vertical active area	-	VDISP	-	1280	-	Line
Vertical Refresh rate	VRR	-	-	60	-	Hz

Note: (1) The VS and VBP pulse width are related to GIP start pulse and GIP clock pulse timing. The GIP start pulse and GIP clock pulse must be set at corresponding position for LCD normal display.

MIPI ID Address :

Page	Address	Value
0xFF, 0x98, 0x81, 0x01	0x00	0x98
	0x01	0x81
	0x02	0x0C

7. *Optical Characteristics*

Item	Symbol		Condition	Min.	Typ.	Max.	Unit	Note
Brightness	Bp		θ=0° Φ=0°	-	350	-	Cd/m^2	
Uniformity	⊿Bp			75	80	-	%	
Viewing Angle	3:00		Cr≥10	-	85	-	Deg	3
	6:00			-	85	-		
	9:00			-	85	-		
	12:00			-	85	-		
Contrast Ratio	Cr		θ=0° Φ=0°	700	800	-	-	4
Response Time	T_r			-	30	40	ms	5
	T_f						ms	
Color of CIE Coordinate	W	x	θ=0° Φ=0°	Typ -0.05	0.320	Typ +0.05	-	1,6
		y			0.335		-	
	R	x			0.632		-	
		y			0.329		-	
	G	x			0.278		-	
		y			0.560		-	
	B	x			0.142		-	
		y			0.136		-	
NTSC Ratio	S			-	55	-	%	

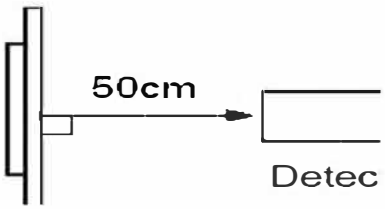
Note: The parameter is slightly changed by temperature, driving voltage and materiel

Note 1: The data are measured after LEDs are turned on for 5 minutes. LCM displays full white. The brightness is the average value of 9 measured spots. Measurement equipment BM-7 (Φ5mm)

Measuring condition:

- *Measuring surroundings: Dark room.*
- *Measuring temperature: Ta=25℃.*
- *Adjust operating voltage to get optimum contrast at the center of the display.*

Measured value at the center point of LCD panel after more than 5 minutes while backlight turning on.

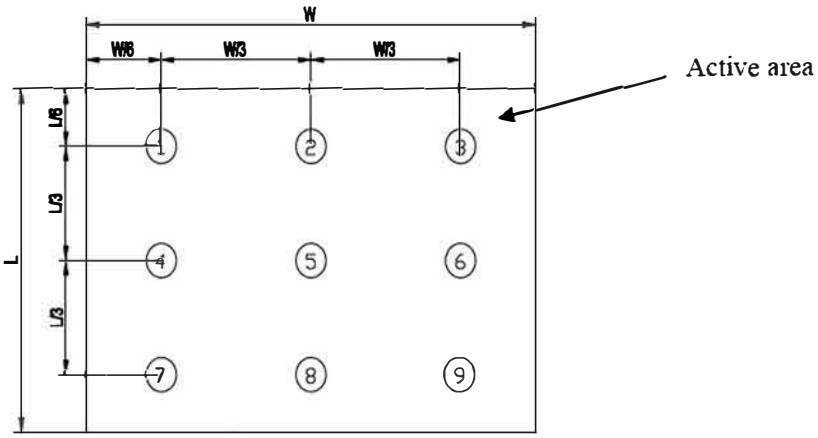


Note 2: The luminance uniformity is calculated by using following formula.

⊿Bp = Bp (Min.) / Bp (Max.)×100 (%)

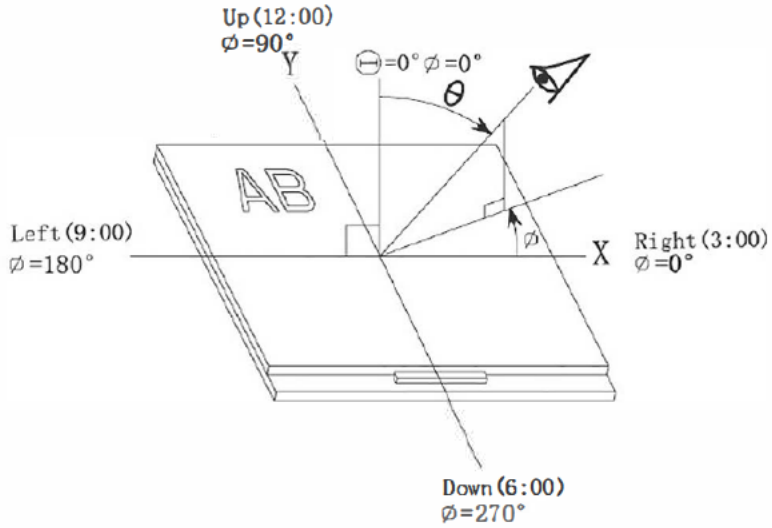
Bp (Max.) = Maximum brightness in 9 measured spots

Bp (Min.) = Minimum brightness in 9 measured spots.

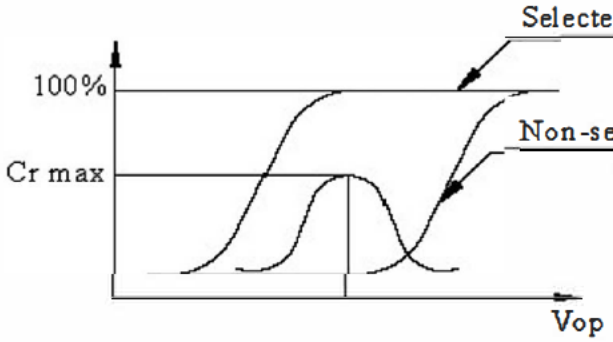


Note 3: The definition of viewing angle:

Refer to the graph below marked by θ and Φ



Note 4: Definition of contrast ratio.(Test LCD using DMS501)



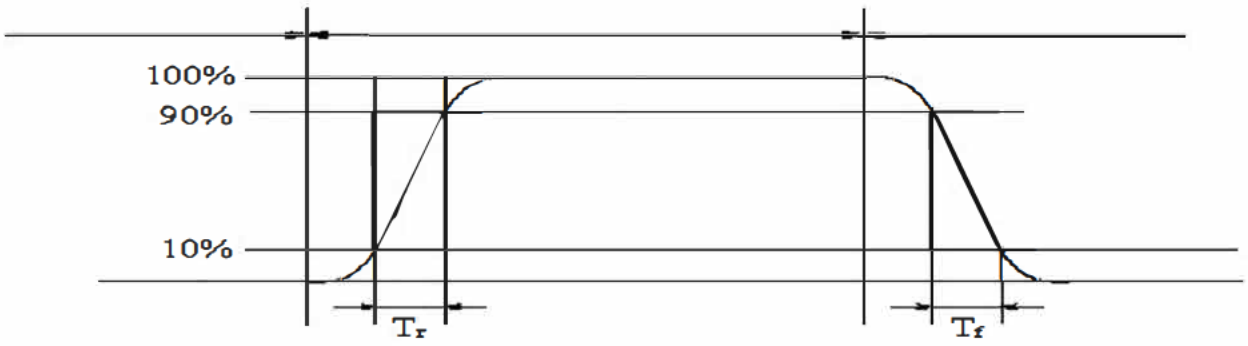
*Conditions

Operating Voltage	:	Vop
Frame Frequency	:	70Hz
Appling Waveform	:	1/N duty 1/a bias
Viewangle (θ, Φ)	:	(0°, 0°)

$$Contrast\ ratio(Cr) = \frac{Brightness\ of\ selected\ dots}{Brightness\ of\ non-selected\ dots}$$

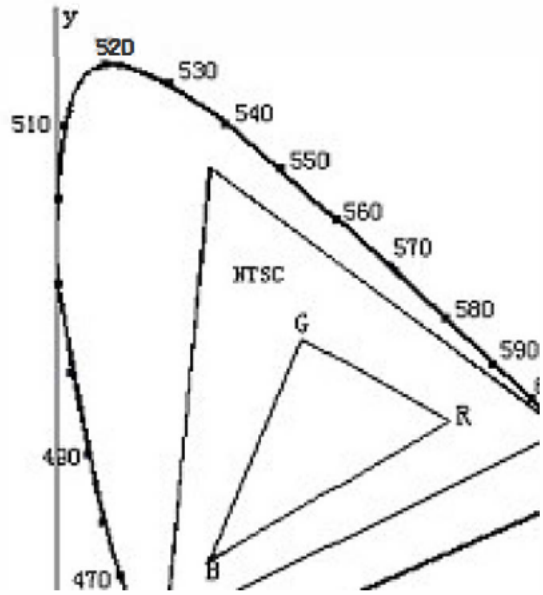
Note 5: Definition of Response time. (Test LCD using DMS501):

The output signals of photo detector are measured when the input signals are changed from"black"to"white"(rising time) and from" white"to "black"(falling time), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes.Refer to figure as below.



The definition of response time

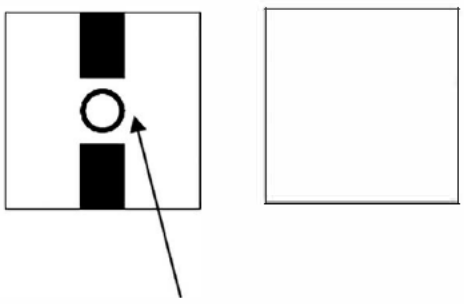
Note 6: Definition of Color of CIE Coordinate and NTSC Ratio.



Color gamut:

$$S = \frac{\text{area of RGB triangle}}{\text{area of NTSC triangle}} \times 100\%$$

Note 7: Definition of cross talk.
*Cross talk ratio(%)=|pattern A Brightness-pattern B Brightness|/pattern A Brightness*100*



Measurement point(center)

Electric volume value=3F+/-3Hex

8. Reliability Test Items and Criteria

Test Item	Test condition	Remark
High Temperature Storage	Ta = 80℃ 240hrs	Note1,Note4
Low Temperature Storage	Ta = -30℃ 240hrs	Note1,Note4
High Temperature Operation	Ta = 60℃ 240hrs	Note2,Note4
Low Temperature Operation	Ta = -20℃ 240hrs	Note1,Note4
Operation at High Temperature/Humidity	+50℃, 90%RH 240hrs	Note4
Thermal Shock	-30℃/30 min ~ +80℃/30 min for a total 10 cycles, Start with cold temperature and endwith high temperature.	Note4
Vibration Test	Frequency range:10~55Hz Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X. Y. Z. (6 hours for total)	
Mechanical Shock	100G 6ms,±X, ±Y, ±Z 3 times for each direction	
Package Vibration Test	Random Vibration : 0.015G*G/Hz from 5-200HZ, -6dB/Octave from 200-500HZ 2 hours for each direction of X. Y. Z. (6 hours for total)	
Package Drop Test	Height:60cm 1 corner, 3 edges, 6 surfaces	
Electro Static Discharge	±2KV, Human Body Mode, 100pF/1500Ω	

Note 1: Ta is the ambient temperature of samples.

Note 2: Ts is the temperature of panel's surface.

Note 3: In the standard condition, there shall be no practical problem that may affect the display function. After the reliability test, the product only guarantees operation, but don't guarantee all of the cosmetic specification.

Note 4: Before cosmetic and function test, the product must have enough recovery time, at least 2 hours at room temperature.

9. *Precautions for Use of LCD Modules*

9.1 Handling Precautions

9.1.1 The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

9.1.2 If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

9.1.3 Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

9.1.4 The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

9.1.5 If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

— Isopropyl alcohol — Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

— Water — Ketone — Aromatic solvents

9.1.6 Do not attempt to disassemble the LCD Module.

9.1.7 If the logic circuit power is off, do not apply the input signals.

9.1.8 To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

a. Be sure to ground the body when handling the LCD Modules.

b. Tools required for assembly, such as soldering irons, must be properly ground.

c. To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

d. The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

9.2 Storage precautions

9.2.1 When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

9.2.2 The LCD modules should be stored under the storage temperature range. If the LCD modules will be stored for a long time, the recommend condition is:

Temperature : *0℃ ～ 40℃*

Relatively humidity: *≤80%*

9.2.3 The LCD modules should be stored in the room without acid, alkali and harmful gas.

9.3 *The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.*

END