DISPLAY SPECIFICATION

Product NO: (产品型号) **IE-Y-2431CS03S-CB-1**
Customer : (客 户) _____

REVISION RECORD

REV NO.	CONTENTS	REV DATE	REMARKS
A	**First Edition**	**2021-08-04**	First Edition

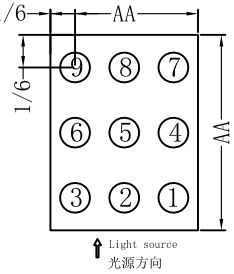
CONTENTS

1. GENERAL INFORMATION

Item 项目	Contents 内容	Unit 单位
LCD Type LCD 类型	ALL TFT，Positive Transmissive type	-
Number of Dots 点阵	240(RGB) *240	Dot
Outline dimensions 外形尺寸	35.7(W)* 39.5(H)*2.94(T)	mm^3
Active area 有效区域	27.72(W)* 27.72 (H)	mm^2
Pixel pitch 像素	0.1155*0.1155	mm^2
Module size 模组尺寸	1.54	inch
Viewing direction 视角方向	ALL	O'clock
Backlight type 背光类型	White LED(3*LED)	-
LCD Driver IC LCD 驱动 IC	ST7789V	-
Interface type 接口类型	MCU8bit interface	-
LCM Input voltage 模组输入电压	2.8±0.1	V

Product Specification

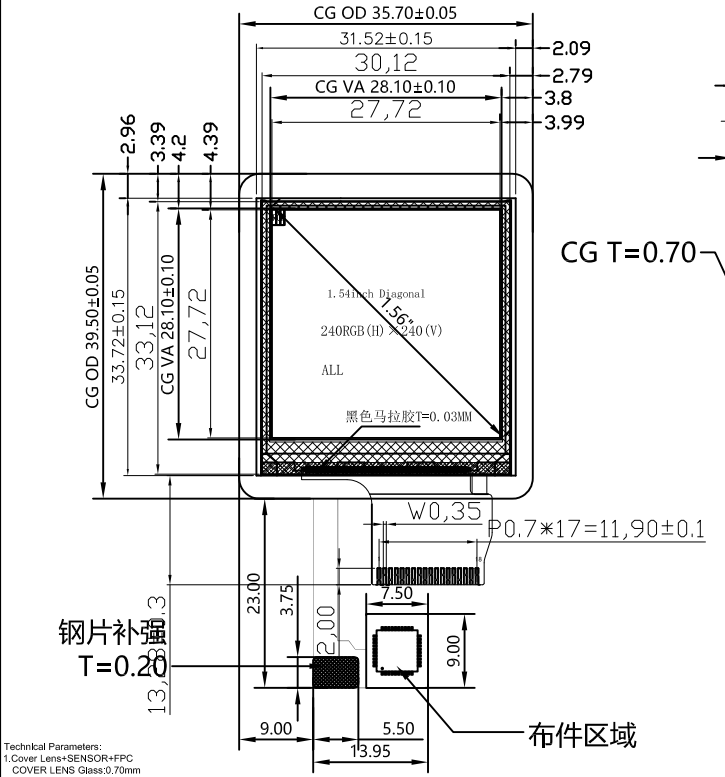
1. 批量产品成品亮度公差为±10% ，测试条件IF=20mA/LED,V=3.0V~3.3V/LED.
2. 批量产品成品色坐标公差为±0.03.
3. 批量产品均匀性80%以上.

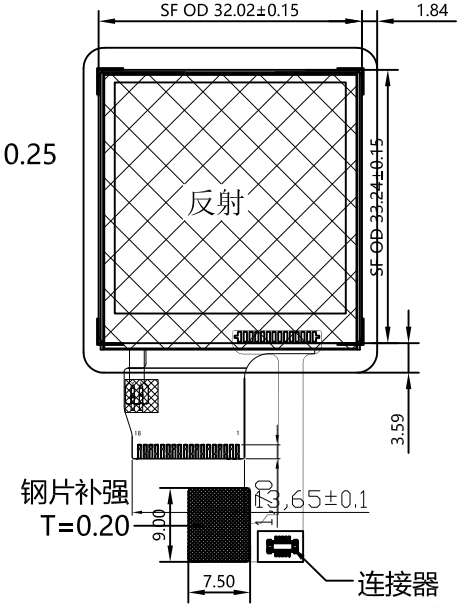


测试距离:500mm
Measure distance:500mm
测量角度:1°,9个点
Angle:1°,9 Points
亮度值是用BM-7色度仪测试
The Measurement instrument is:BM-7
均匀性=最小/最大亮度值*100%
Uniformity=min/max*100%

设计注意事项：
1. 图中FRAME VA为推荐TP视窗位置、大小，建议TP视窗位置、大小不要超过FRAME VA。
2. 整机机壳带泡棉产品，建议客户机壳泡棉进入LCD单边0.5MM MIN,防止漏光。
3. 整机机壳不带泡棉产品，建议客户整机TP的丝印黑油开窗或者LENS丝印黑油开窗比LCD A.A区单边大0.6MM MAX。
4. 客户需保证触摸屏下表面到玻璃上表面最少0.3MM MIN(非贴合)。

技术要求:
1) 液晶显示模式: 1.54″TFT transmissive
2)视角：ALL
2) 显示颜色：262K COLORS
3) 点阵：240*240
4)驱动芯片型号:ST7789V
5)工作温度:-20° -----70°
储存温度:-30° -----80°
6)未注尺寸公差:±0.2mm
7)材料及工艺符合 ROHS



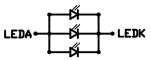


LCM	
PIN	Define
1	TE
2	VCC
3	CS
4	RESET
5	RS
6	WR
7	RD
8	D7
9	D6
10	D5
11	D4
12	D3
13	D2
14	D1
15	D0
16	GND
17	LEDK
18	LEDA

TP_FPC	
PIN	NAME
1	GND
2	VDD
3	SCL
4	INT
5	SDA
6	RST
7	NC
8	NC
9	NC
10	NC

Technical Parameters:
1.Cover Lens+SENSOR+FPC
COVER LENS Glass:0.70mm
ITO SENSOR Film: 0.25mm
Lead wire: FPC
Total thickness: 0.95±0.10mm
IC: FT6336G (single point + gesture)
2. Working voltage: 2.8V-3.3 V
3. Light transmittance: ≥82%
4. Surface hardness: 6H
5. Working environment: -20℃~+70℃, ≤90%RH
6. Storage environment: -30℃~+80℃, ≤90%RH
7. Dimensions without tolerance: ±0.10,
8. Unremarked chamfering ±0.15

组装方式：	机器组装	
模组接口方式：	MCU 8BIT	
01	首次出图	
02		
03		
04		
05		
06		



LED CIRCUIT DIAGRAM

TITLE: ASSEMBLY	DO NOT SCALE THIS DRAWING, GENERAL TOLERANCE:±0.2				
PART NO.:				MODULE NO.:	00
DRAWN BY:		DATE:		PROJECTION:	
CHECKED BY:		DATE:		SCALE:N.T.S	UNIT: mm
APPROVED BY:		DATE:		SHEET: 1 OF 1	

3. INTERFACE DESCRIPTION 接口定义

LCD PIN DEFINITION

NO.	PIN NAME	Description
1	**TE**	TE PIN
2	**VCC**	Power Supply 2.8V Voltag
3	**CS**	Input pin for chip selection signal
4	**RESET**	LCM Reset input signal
5	**RS**	Register selection signal
6	**WR**	Read strobe signal input pin
7	**RD**	Read signal
8~15	**DB7-DB0**	Display Data I/O
16	**GND**	Ground
17	**LEDK**	LED Cathode
18	**LEDA**	LED Anode

CTP PIN DEFINITION

NO.	PIN NAME	Description
1	**GND**	Ground
2	**VDD**	Power supply(2.8V)
3	**SCL**	IIC Serial interface Clock input
4	**INT**	External interrupt to the host
5	**SDA**	IIC Serial data input/output PIN
6	**RST**	Reset Signal pin (“Low” is enable)
7	**NC**	Not connect
8	**NC**	Not connect
9	**NC**	Not connect
10	**NC**	Not connect

4. ABSOLUTE MAXIMUM RATINGS
极限参数(IC)

Parameter 参数	**Symbol** 符号	**Min** 最小值	**Max** 最大值	**Unit** 单位
Supply voltage for logic 逻辑电压 I/O	IOVCC	-0.3	+4.6	V
Input voltage for analog circuit 输入模拟电压	VCC	-0.3	+4.6	V
Operating temperature 操作温度	TOP	-20	+70	˚C
Storage temperature 存储温度	TST	-30	+80	˚C
Humidity 湿度	RH	-	90%(60˚C)	RH

5. ELECTRICAL CHARACTERISTICS
模块电气特性

Parameter 参数	Symbol 符号	Min 最小指	Typ 典型值	Max 最大值	Unit 单位
Analog operating voltage 模拟电压	VCC	2.4	2.75	3.3	V
Logic operating voltage 逻辑电压	IOVCC	1.65	1.8	3.3	V
Input voltage “H”level 输入高电平	V_{IH}	0.7 *IOVCC	-	IOVCC	V
Input voltage “L”level 输入低电平	V_{IL}	GND	-	0.3* IOVCC	V
Output voltage “H”level 输出高电平	V_{OH}	0.8*IOVCC	-	IOVCC	V
Output voltage “L”level 输出低电平	V_{OL}	GND	-	0.2 *IOVCC	V

6. BACKLIGHT CHARACTERISTICS

背光电气特性

Item 项目	Symbol 符号	Min 最小值	Typ 中间值	Max 最大值	Unit 单位	Condition 条件
Forward voltage 正向电压	Vf	3.0	-	3.3	V（伏）	If=60mA, Ta=25℃
Number of LED LED 灯数	-	3			Piece （颗）	-
Connection mode 连接类型	S/P	Series and Parallel（3 灯并联）			-	-

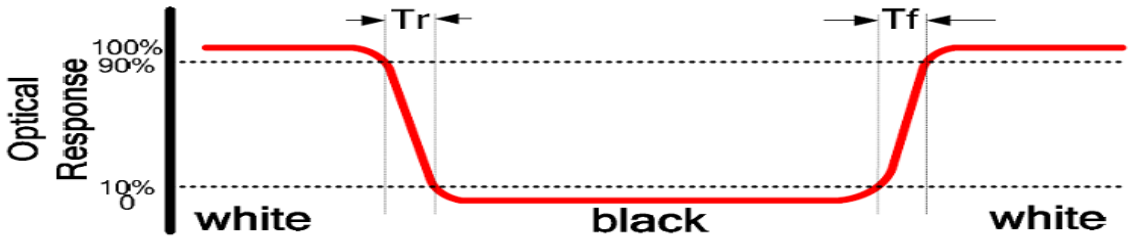
7. OPTICAL CHAYACTERISTICS

光学特性

Item 项目	Symbol 符号	Condition 条件	Min 最小值	Typ 典型值	Max 最大值	Unit 单位	Remark 注释	Note 备注
Response time 响应时间	Tr+Tf	Θ=0° Ø=0° Ta=25˚C	-	30	-	ms	FIG1	1
Contrast ratio 对比度	Cr		-	800	-	-	FIG2	2
Color gamut 饱和度	S(%)			60	-	%	-	-
Luminance uniformity 均匀度	δWHITE		-	80	-	%	FIG2	3
Viewing angle range 视角范围	Θx+	CR≧10 Ta=25˚C	-	80	-	deg	FIG3	4
	Θx-		-	80	-	deg	FIG3	
	Θy+		-	80	-	deg	FIG3	
	Θy-		-	80	-	deg	FIG3	
LCM 亮度	Lv	Θ=0° Ø=0° Ta=25˚C	-	300	-	Cd/m^2	FIG2	5
CIE (X,Y) Chromaticity 色度坐标	White(X)		-	TBD	-	-	FIG2	6
	White(Y)		-	TBD	-	-		

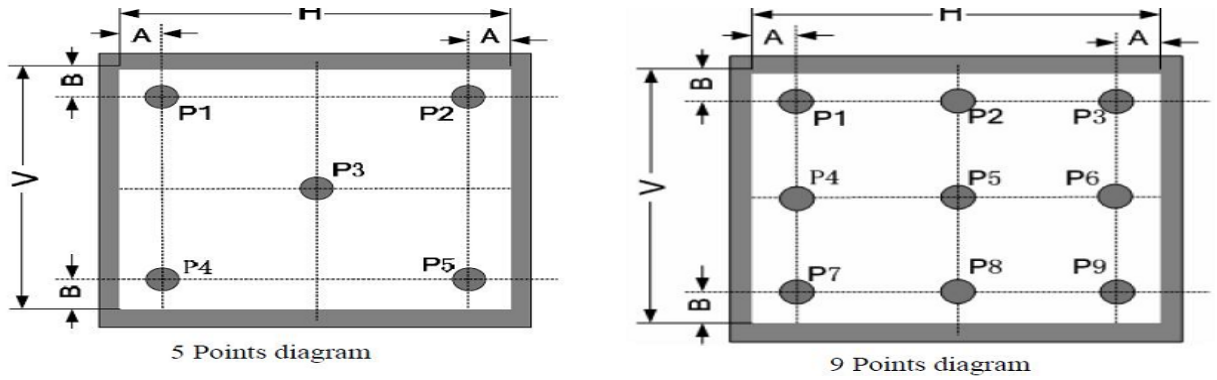
Note1.Response time is the time required for the display to transition from White to black(Rise Time,Tr)and from black to white(Decay Time,Tf).For additional information see FIG1...

FIG1. The definition of Response time



Note2.contrast Ratio(CR) is defined mathematically by the following formula ,For more information see FIG2.
Contrast Ratio(CR)=Average Surface Luminance with all white pixels/ Average Surface Luminance with all black pixels

FIG2. Measuring method for Contrast ratio,surface luminance,Luminance uniformity,CIE(X,Y) chromaticity.

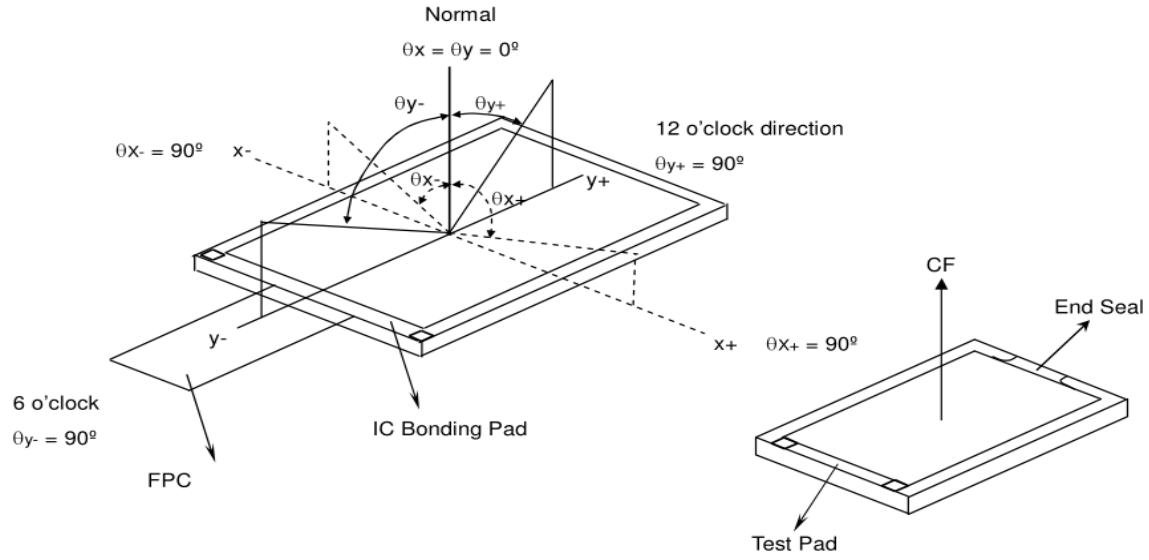


Note3.The uniformity in surface luminance(WHITE) is determined by measuring luminance at eath test position,and then dividing the maximum luminance of all white pixels by minimum luminance of all white pixels,For more information seeFIG2.
WHITE=Minimum Surface Luminance with all white pixels(P1,P2,.....)/Maximum Surface Luminance with all white pixels(P1,P2,.....)

Note4.Viewing angle is the angel at which contrast ratio is greater than a specific value.For TET module,the specific value of contrast ratio is 10.For monochrome and color stn module,the specific value of contrast ratio is2.The angles are determined for the horizontal or x axis and the vertical or

y axis with respect to the z axis which is normal to the LCD surface.For more information see FIG3

FIG3 The definition of viewing angle



Note5. Surface luminance is the LCD surface luminance with all white pixels,For more information see FIG2.
LV=Average Surface Luminance with all white pixels(P1,P2,.....)

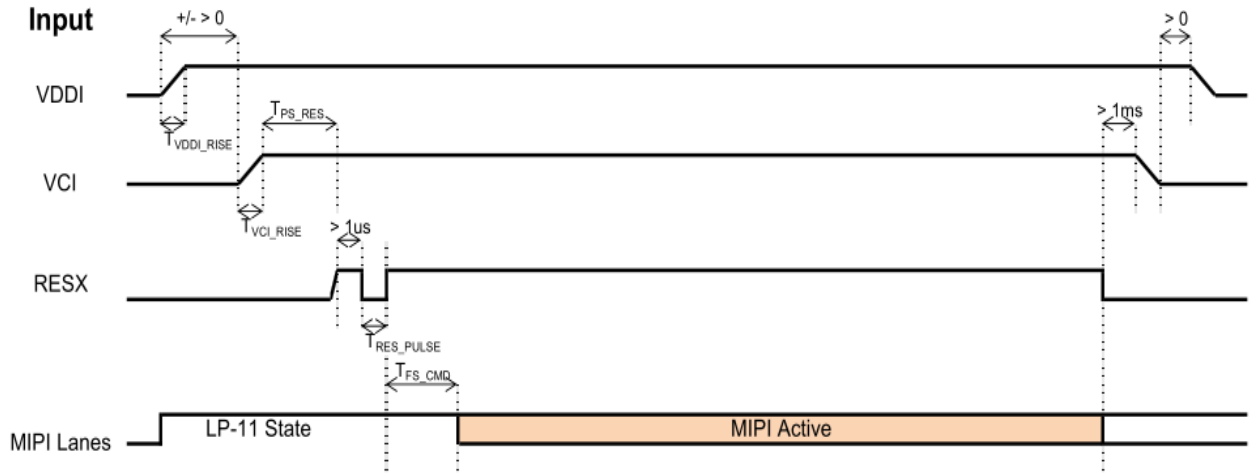
Note6.CIE(X,Y)chromaticity is the Center point value.For more information see FIG2.

Note7.For Viewing angle and response time testing,the testing date is base on Autronic-Melchers' s ConScope.Series instruments.For contrast ratio,Surface Luminance,Luminance uniformity and CIE,the testing date is base on CS-2000(BM-7/CA310) photo detector.

Note8.For TN type TFT transmissive module,Gray scale reverse occurs in the direction of panel viewing angle

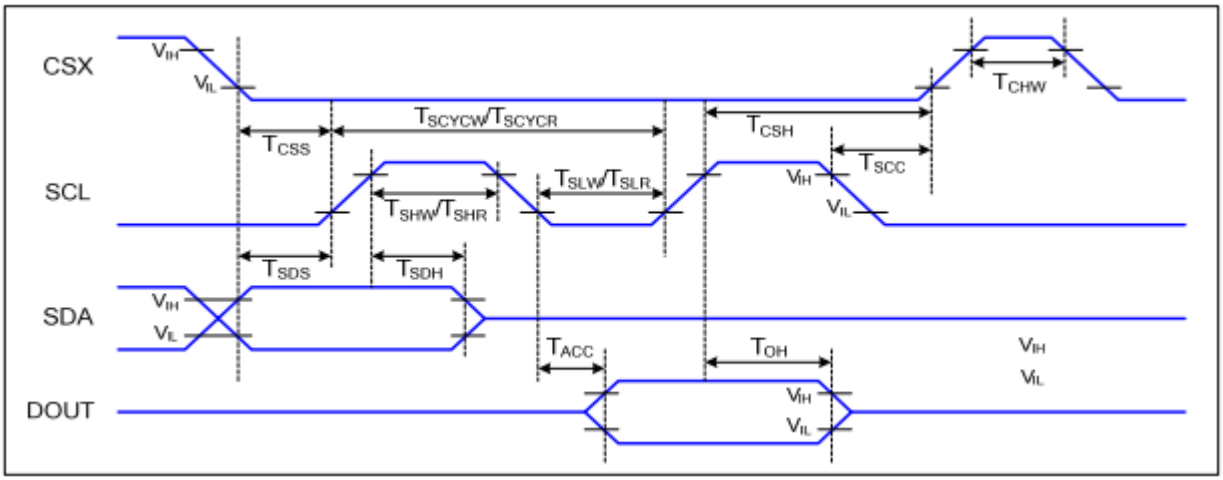
8. **Recommended Operating Sequence**

8.1 Power on/off sequence with 2- power



Symbol	Characteristics	Min.	Typ.	Max.	Units
T_{VDDI_RISE}	VDDI Rise time	20	-	-	us
T_{VCI_RISE}	Case A: VCI Rise time	200	-	-	us
	Case B: VCI Rise time	40			
T_{PS_RES}	VDDI/VCI on to Reset high	5	-	-	ms
T_{RES_PULSE}	Reset low pulse time	10	-	-	us
T_{FS_CMD}	Reset to first command	10	-	-	ms

8.2 Power on/off sequence with 3- power



Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	
	T_{SHW}	SCL "H" pulse width (Write)	15		ns	
	T_{SLW}	SCL "L" pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

NOTE: This section is only for reference,Details please refer to the IC specification.

9. RESET INPUT TIMING

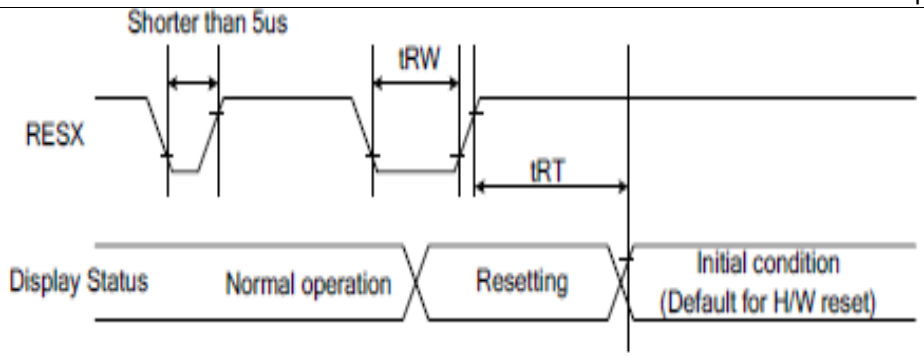


Figure 126: Reset Timing

Table 47: Reset Timing

Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

Notes:

1. *The reset cancel also includes required time for loading ID bytes, VCOM setting and other settings from EEPROM to registers. This loading is done every time when there is H/W reset cancel time (tRT) within 5 ms after a rising edge of RESX.*
2. *Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the Table 48.*

Table 48: Reset Descript

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

3. During the Resetting period, the display will be blanked (The display enters the blanking sequence, which maximum time is 120 ms, when Reset Starts in the Sleep Out mode. The display remains the blank state in the Sleep In mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection can also be applied during a valid reset pulse, as shown below:

NOTE: This section is only for reference,Details please refer to the IC specification.